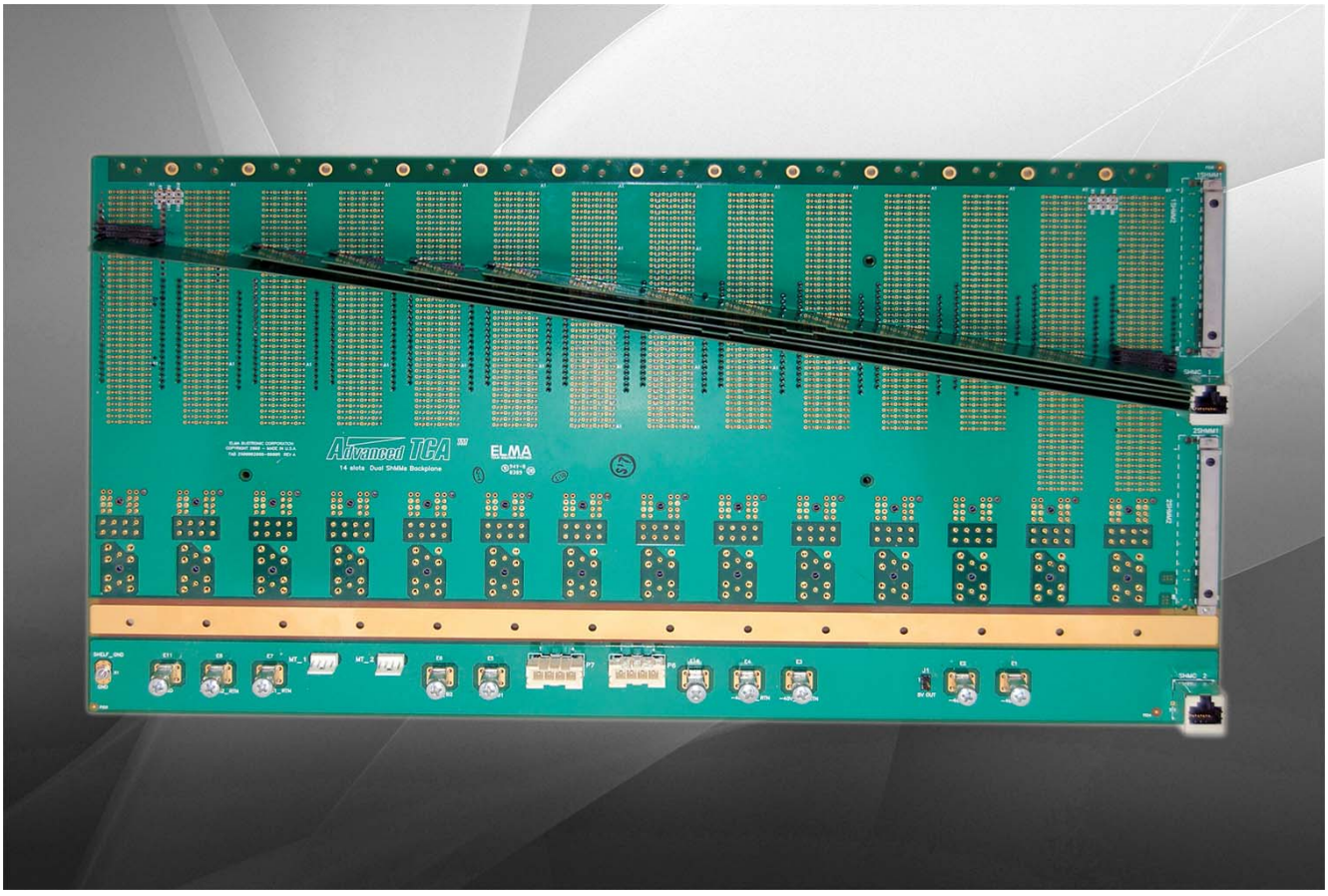
≠ Z-Plane™

A Complete Systems Approach for High Speed Backplanes



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The demand for increased digital data throughput is fueling the quest for higher speeds in datacom and telecom systems. The critical elements of these systems are the modular backplane, including its multilayer printed circuit board backplane, and the daughter cards, also known as line cards or blades. Data rates for these systems are rapidly approaching 40 GB/s across a standard backplane, with active work being done to achieve speeds up to 100 GB/s. This means that data rates of 10 and 25 GB/s will be required for each signal pair. Systems which use this type of construction are telecom switches, digital cross-connects, storage subsystems, routers, embedded platforms, and blade servers. The system design is such that by adding or changing the line cards these systems can be upgraded without complete system replacement. Since the modular backplane has the longest life of the key components in these systems, extended backplane performance can lead to an even longer life cycle. In order to meet future industry needs, it is desirable that the modular backplane be scalable with regard to the line card speeds, while maintaining compatibility with legacy equipment and connector interfaces.

The two-dimensional nature of the multilayer printed circuit backplane is a potential bottleneck for data throughput speeds. The signal integrity problems which limit bandwidth include signal attenuation, system noise (crosstalk), pulse distortion, and pulse skew. The fine gauge signal lines required for routing circuitry through a multilayer board backplane are one cause of these problems. Trace widths, thickness, as well as the printed circuit board insulating materials have a direct impact on conductive and dielectric losses. Conductor spacing, impedance mismatches, and shielding are related to crosstalk performance and signal paths interact with the ground and power network within the multilayer board in unpredictable and problematic ways.

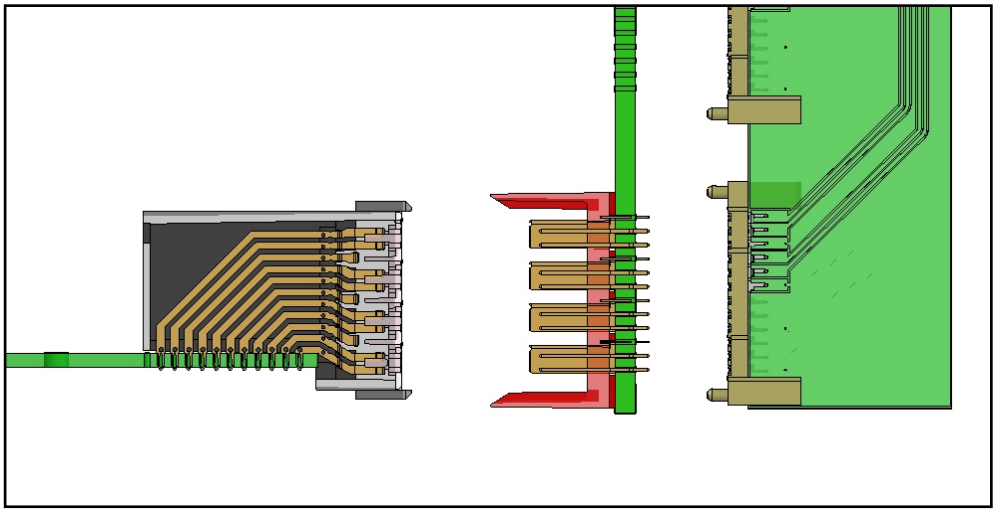
The plated-through holes or “vias,” which connect the various layers of a printed circuit board, are used for connector terminations and are another source is signal integrity problems. The size and spacing of the vias typically required by connectors can lead to impedance mismatches, which in turn can cause signal reflections and crosstalk. An even greater problem is circuit “stubs,” which arise when a portion of the plated-through hole is not terminated. That is, a typical via has circuit elements connecting at both ends of the hole, and when this does not occur, a circuit “stub” results. A “stub” causes resonances and reflections, seriously limiting the bandwidth.

There are a number of potential improvements which can be made to the design of the backplane circuit boards. Signal attenuation is addressed by using advanced printed circuit board dielectrics such as Megtron 6, Nelco 4000-13, and Rogers 4350. These materials have lower dielectric losses than the more typical FR4 epoxy/glass laminate materials. Back-drilling of vias is the conventional method used to minimize or remove circuit stubs by removing the excess material length not terminating to a circuit. Currently, new connector designs, with increased density and smaller vias are being introduced. Signal conditioning technologies including equalization circuits and signal pre-emphasis are being employed to improve signal speed.

These technologies are not without their own sets of compromises and problems. New materials can raise the cost of the printed circuit board materials. Some of these materials require special fabrication methods and reliability may be compromised. Back-drilling and special via designs further add to fabrication costs. Signal conditioning leads to increased crosstalk and electro-magnetic-interference

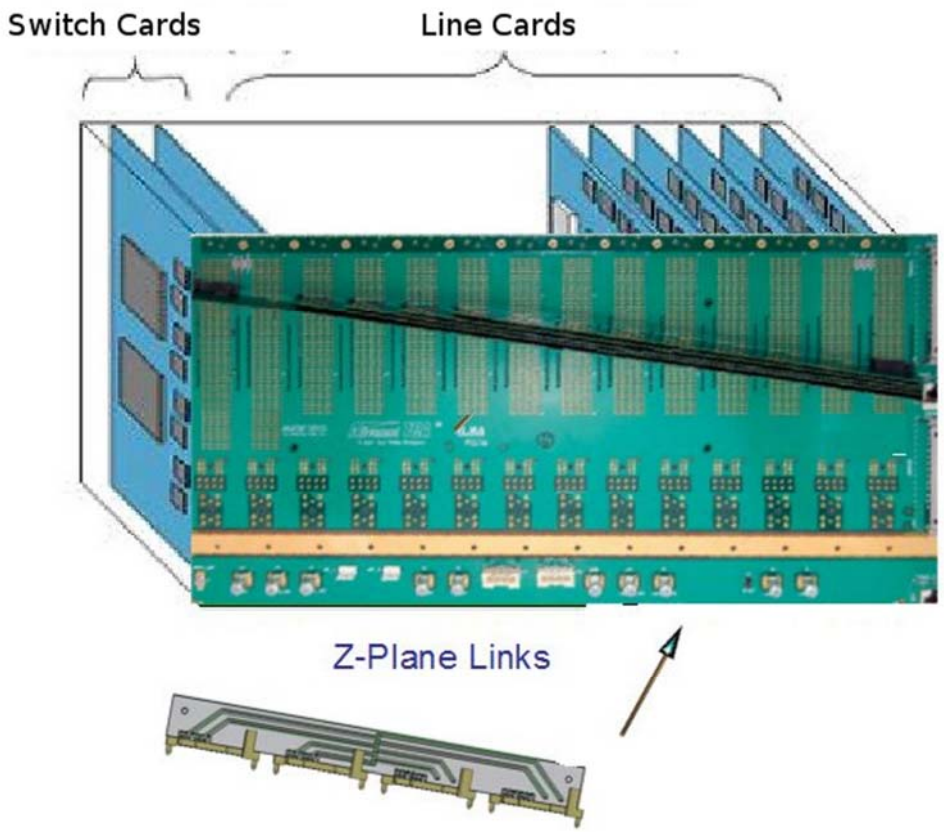
(EMI), and contributes to increased power usage while the extra heat generated exacerbates thermal management problems as well as adding cost. In addition, some new connectors are less robust than their predecessors, and they use high aspect ratio plated through holes, requiring costly state-of-the-art drilling and plating.

Z-Plane offers an alternative to conventional printed circuit technology. It is a full systems approach which takes into account a variety of complex factors including engineering, manufacturability, scalability, and legacy issues. Instead of the conventional multiple signal layers stacked between ground planes with the connector terminals perforating those layers, the Z-Plane high-speed signals are routed from connector to connector on narrow two-layer printed circuit board (PCB) links. These links run across a typical backplane in a plane normal to its flat rear surface – the Z-Plane.



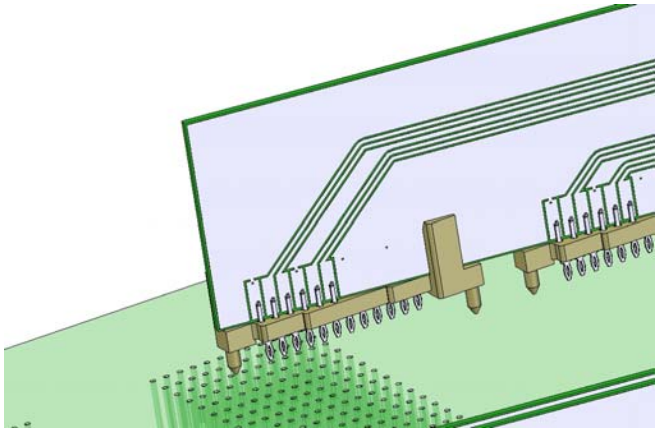
Z-Plane X-Section

The links are linear circuit elements with well defined electrical characteristics. In point-to-point serial systems, the PCB links run at an angle which is related to the connector and slot pitch and interconnects the various high-speed signal points of a meshed network.



Z-Plane ATCA Backplane

The matched impedance interconnection is made between the narrow PCB link and the backplane using a connector or adapter, which also orients the narrow PCB link to accommodate the specific angle required for the interconnection to the elements of the network.



Z-Plane Adapter and PCB Links

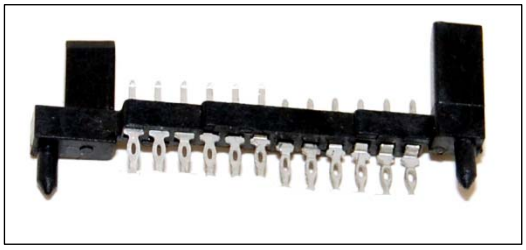
Circuit stubs are eliminated by making a direct connection to the backplane connector either by an extended pin or a plated through hole. The Z-Plane Link circuit construction may use either microstrip or stripline circuitry. However, microstrip has been generally used because of the low losses inherent in this form. The conductor widths and pitch are not constrained, so conductive losses can be minimized. Conductor spacing is also not constrained, allowing for shielding and circuit spacing which can further reduce crosstalk. Low-loss dielectric materials may be used selectively, as required, for the longer length, higher loss channels without seriously impacting the final cost.

The Z-Plane technology is capable of being adapted to a variety of custom backplane designs and standards. Nevertheless, the initial model for developing the routing format for the Z-Plane system is based on the mesh topologies of the PICMG 3.0, Advanced TCA specification. Both the Dual Star and Full Mesh topologies have been analyzed. At first glance, interconnecting to this complex system was daunting, since the circuitry appeared to be too complex to accept a simple linear interconnect. However, the mesh topologies are very regular configurations and readily lend themselves to this design approach.

The Dual Star fabric represents one of the most commonly used and simple forms of signal routing. In this configuration, every card slot on the backplane is connected to two “hub” cards. Each link has two circuit “levels” with each level interconnecting to the specific card slot and to two “hub” slots. There are redundant links for each channel. The angle at which the link traverses the backplane is defined by the physical hardware and is determined by the connector slot pitch and the spacing of the connector rows. Each level of the link is terminated with a Z-Plane Adapter, which directly interconnects to the appropriate pins of the backplane connector on the rear of the backplane.

The Full Mesh fabric is an extension of this scheme and requires additional circuit “levels.” The full mesh system will require four levels of Z-Plane circuitry, with the balance of the shorter interconnects being accommodated by the multilayer board. Many custom configurations are also possible including straight, right-handed, left-handed, and crossover adapters.

The use of Z-Plane technology will extend the life of the existing connector systems, such as the ADF connector family, well beyond their normal limits, since most of the signal integrity issues of these connectors reside in the printed circuit board interface (i.e., vias). The direct matched impedance connection to the header provided by the Z-Plane link eliminates many of the common problems.



Z-Plane Adapter

The adapter for the Z-Plane interconnection system has a short impedance matched connection between the pin and the backplane connector. The adapter contacts are a simple design, with solder tabs at one

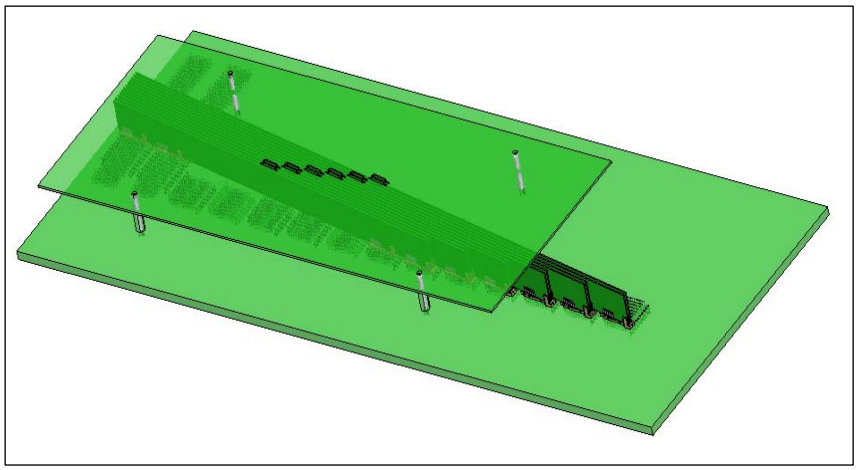
end, which connect to the link, and a press-fit termination at the other end, either a press-fit pin or a compliant contact bent at a right angle to accept a pin from the backplane connector projecting through the rear of the backplane. The press-fit pin is used for thicker backplanes (0.132" thick and greater) and uses the plated through hole for the press-fit connection to the backplane connector, whereas the connector with the compliant hole can be used with thinner structures (0.093" thick or less).

The alignment pegs on the adapter housing function as positioning guides during assembly and provide strain relief for the adapter. Strain relief between the Z-Plane Link printed circuit board and the adapter is provided by tabs which project vertically from the base of the adapter.

The adapter housing and terminals have been designed such that the long axis of the Z-Plane Link is at an angle relative to the normal axis of the backplane, so that the appropriate interconnection can be made to the high-speed signal lines on the daughter cards of the system. The adapter has staggered arrays so they can be stacked adjacent to one another and mate with the backplane connector.

Once the adapters are soldered to the link, the Z-Plane Link assembly is simply pressed into place, using tooling similar to that used for standard press-fit connectors.

In addition, the Links may be fitted with a simple protective cover platen to prevent damage during handling or for applications requiring ruggedized designs. The small tabs on the top of each Z-Plane Link fit into slots on the cover platen to precisely locate and secure the Links.



Z-Plane Links with Protective Platen

The adapter press-fit pin connection to the printed circuit board has high normal force contacts which have a history of excellent reliability. The "eye of the needle" termination design is a mainstay of the backplane manufacturing industry. The new compliant-hole contact should have a similar performance profile to the press-fit pin, since it has high wipe combined with high contact normal force.

The solder joints between the link PCB and the adapter are made using standard soldering processes or standard surface mount technology (SMT) soldering processes. The parts are easily handled and do not require special manufacturing technology.

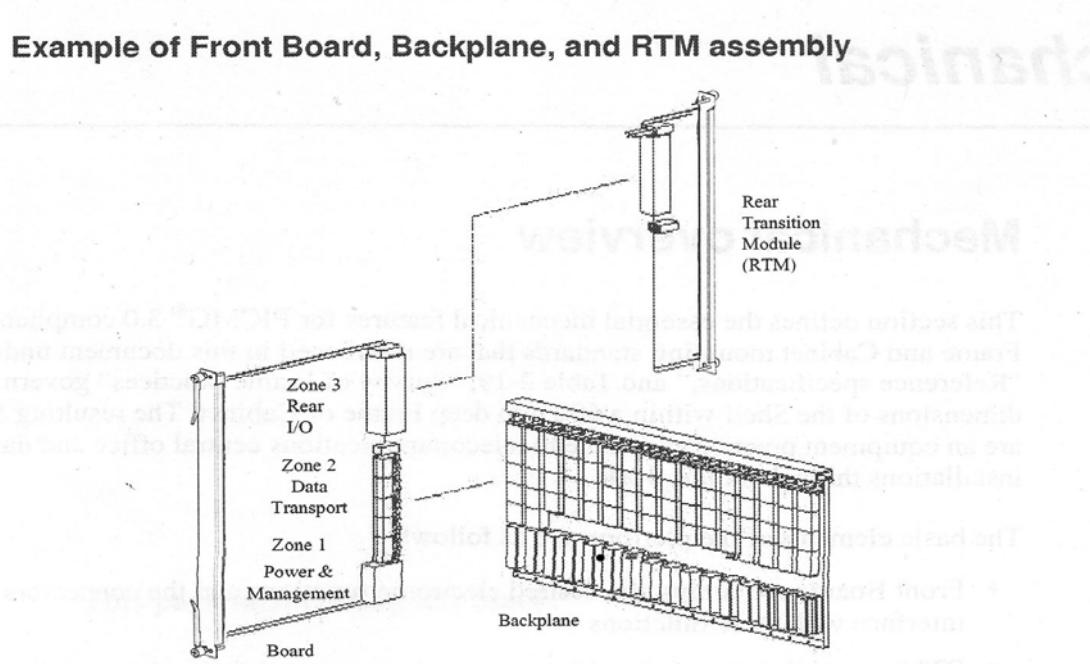
The Z-Plane Links replace the current connections between the traces and the plated through holes (vias). Historically, the current connection points are subject to failure caused by thermal stress and manufacturing problems, such as epoxy smear. Back drilling the vias can add additional reliability problems caused by metal chips and stressing the barrel of the plated-through hole. In cases where the circuit is damaged, in the Z-Plane case the Link can be readily replaced, whereas with current technology a damaged via cannot be replaced and the entire expensive backplane is lost.

The engineering of a standard backplane is a complex task, since it involves iterative processes of measurement, simulation, modeling and prototyping. It is difficult to predict the complex interactions of the complex network of signal, ground and power interconnections. Z-Plane separates the signal structure from the power and ground structures, improving high-speed signal performance, while simplifying analysis and design. The Z-Plane Link may be viewed as a stand-alone component, which can be designed independently from the rest of the system.

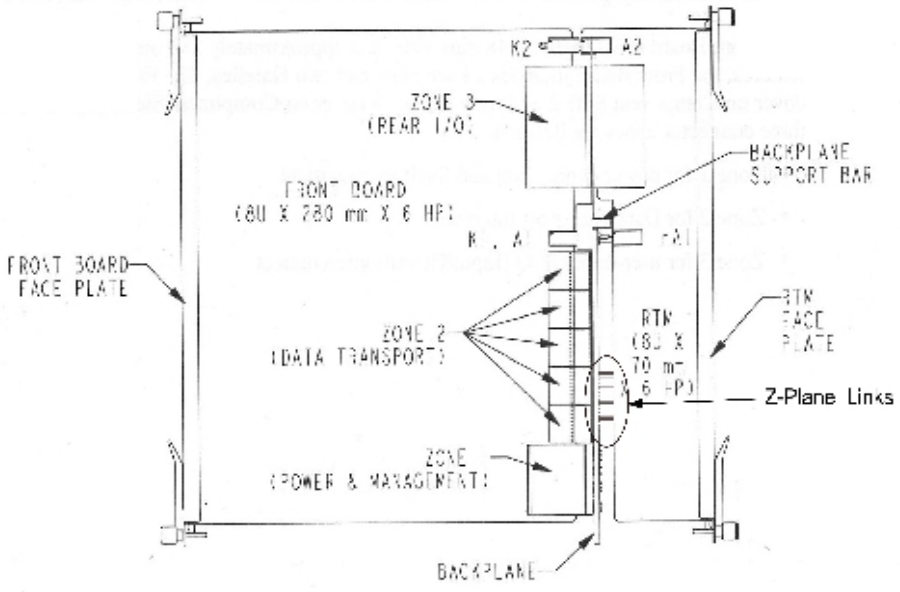
The Z-Plane engineered standard circuit elements have other advantages. New materials and processes can be introduced with much less technical risk, and prototyping of new systems is simplified. Once a single Link is characterized, it only requires different lengths to build an entire system. In comparison, the development of a standard multi-layer board may require complete re-engineering with each design cycle. The Z-Plane system is scalable in configuration, size and performance. The design of a Link can be replicated and reused. This leads to reduced product cycle times and lower overhead costs.

Z-Plane Links

The PICMG 3.0 AdvancedTCA (Telecommunications Architecture) specification was chosen for the initial product development and technology demonstration. It is a common platform developed by the PICMG, and it is aimed at the communications network infrastructure. Because it is an open standard, it enjoys widespread use in many technology segments from industrial internet applications to government and military applications. There is active interest within the ATCA community to increase the data rate from 2.5 GB/s per signal pair to 10 GB/s per signal pair. The intent of this project is to adapt the Z-Plane concept to ATCA applications making minimal changes to the ATCA specification.



The focus of the Z-Plane project is the "data transport" section and the dual star topology. "ADF" type connectors are to be used, along with FR4 printed circuit board material. The purpose is to determine manufacturing feasibility and cost effectiveness, as well as the technical performance of the system.

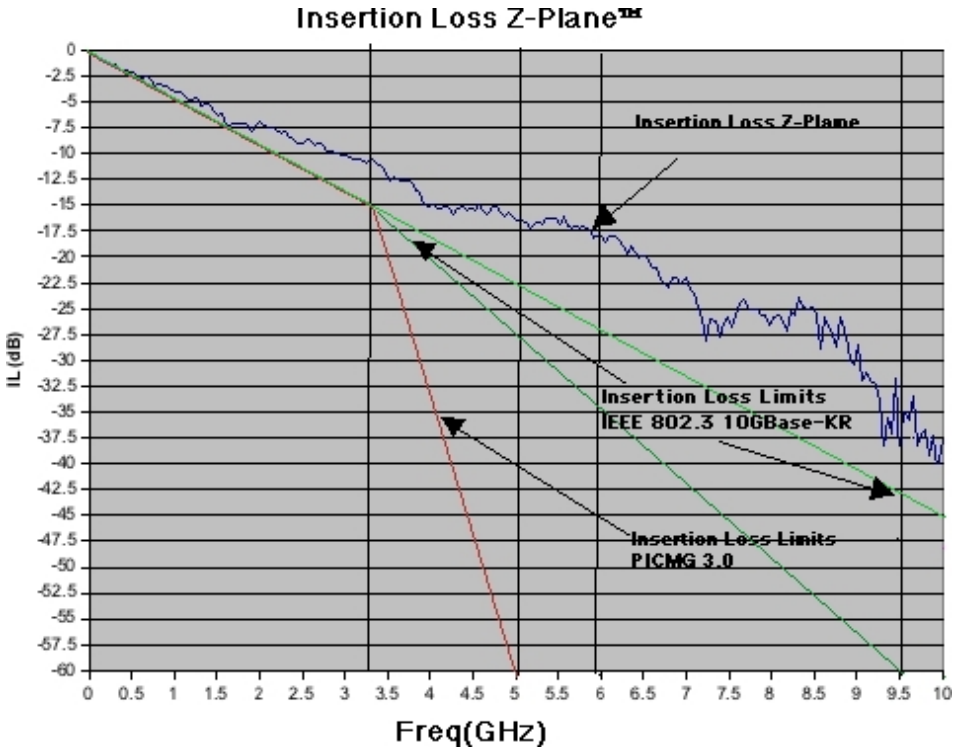


Z-Plane Links installed on an ATCA Backplane

A 14 slot Dual Star configuration with hub slots at one edge of the board was chosen as the model. This is a popular configuration and has the longest signal path for Z-Plane signal integrity evaluation. Two different board types and termination adapters have been evaluated. A relatively thin board (0.092") was evaluated. It used a termination adapter which connected to a pin projecting through the backplane. The second design used a backplane of more conventional thickness (0.134") and was chosen for the mechanical stiffness required for backplane assembly. The Z-Plane adapter terminates to the plated-through hole (via) of the backplane with a press-fit pin termination. This design was chosen because it represents the least physical change. A commercial quality backplane with the high-speed circuitry layers removed was supplied by Elma Bustronic.

The Z-Plane application was a "hybrid" system, in which the six longest channels were Z-Plane Links, with 12 Links per backplane. For the Z-Plane application, a minimum of at least a 6 or 8 layer printed circuit board is required to support the control circuitry and the shorter channels. In comparison, the standard dual star board contains 18 layers.

Although the evaluation of the developmental model is an ongoing process, there are a number of conclusions which can be drawn from the evaluation project. The thin board (0.092") was the first board to be evaluated. In this case, the daughter test card used standard technology and included standard via interconnects to determine the potential effect of using this technology with the modified backplane. The data generated from the attenuation, crosstalk, and TDR measurements indicates that the system will meet if not exceed the IEEE 802.3ap requirements for the 10GB/s backplane.



Z-Plane Insertion Loss on 0.092" Backplane

The thick board (0.134”) has standard lower impedance terminations to the backplane, but is otherwise well matched, and this too will meet or exceed the requirements.

The assembly methodology of the Z-Plane link to the backplane has been evaluated. The parts were assembled to the backplane without damage. The resulting structure was stable and was enhanced as additional links were assembled to the backplane. Fixtures, similar to those used for inserting the standard backplane connectors, will be required to press the links into the backplane, since it is important to keep the link perpendicular to the backplane during assembly. Connector-to-connector length tolerance is accommodated by taking advantage of a slight bow designed into the link. The Z-Plane backplane system can be assembled using standard manufacturing technology and should not pose any special problems.

Several different designs of Z-Plane Links have been evaluated in reference to the specification. The Links can be designed as single, double, or four layer Links with 1, 2, or 4 channels per Link. The 2 layer Link can be used with the dual star configuration to connect two slots on either end. The 4 layer Link is designed for a hybrid full mesh system.

Cost estimates for the Z-Plane backplane as compared to the existing technology have been established. The cost analysis is based on an 18 layer, 14 slot dual star ATCA backplane, as compared to an 8 layer Z-Plane backplane assembly, where the eight longest channels use Z-Plane Links.

Cost Assumptions

Type	Size (w x l)	Thickness	Mat'l	# layers	# back drilled	ZPL links
Standard	9.38” x 17.5”	0.132”	FR4	18	400	n. a.
Z-Plane	9.38” x 17.5”	0.092”	FR4	8	100	16

Estimated Costs

Type	PCB	Back drill	Z-Plane Links *	Total Cost	Est. GB/s
Standard	$435.00	$20.00	n. a.	$455.00	2.5 – 5.0
Z-Plane	$200.00	$ 5.00	$166.00	$371.00	10 - 15

*assembly included

The cost of a Z-Plane backplane is about 20% less than a similar standard FR4 backplane, whereas the data rate of a Z-Plane backplane is approximately 2-3 times higher. High speed versions of the standard configuration will require more costly circuit board materials and manufacturing processes. In order to make a clear comparison, preliminary analysis suggests a standard backplane constructed

with high-speed materials will cost at least $555 ($100 more) when compared with the Z-Plane cost estimates above, giving Z-Plane a 33% cost savings.

Some versions of the Z-Plane system will provide for field upgrades to even higher system throughput. The manufacturing yield of the Z-Plane system will be higher than the standard multilayer board. Engineering costs will be reduced, because the links are reusable as standard components. Signal conditioning technology will be used less, minimizing energy consumption. Z-Plane will also reduce energy costs and materials usage, and consequently, their associated costs will be lower.

The low-loss, impedance controlled signal path has been designed to accommodate bandwidths beyond 10GB/s. The new system design concept emphasizes low-cost as well as compatibility with legacy systems and component design. Although the technology can be adapted to a variety of custom applications, the initial project is focused on PICMG 3.0 (Advanced TCA) and is intended to be compliant with the IEEE 802.3ap 10GBASE-KR standard. Preliminary test data shows that the system can perform beyond 15 GB/s using standard FR4 substrates and conventional manufacturing technology. The selective use of advanced material technology, along with connector design improvements should take the data rates of the Z-Plane system beyond 20 GB/s in its next generation design, without seriously impacting cost.

The Z-Plane interconnection system, using evolutionary technology, promises revolutionary improvements in data throughput and cost. The Z-Plane system provides a practical approach to solving the problems of high bandwidth electronic packaging, using conventional materials, processes and connector designs. It not only improves the system speed and performance, but it can reduce engineering, materials, manufacturing, energy and operating costs. Z-Plane can accommodate a variety of network configurations including legacy systems and is scalable well into the future.

Acknowledgments

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